UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/808,287	03/25/2004	Kenji Kamada	XA-10061	5093

181 7590 04/04/2007

MILES & STOCKBRIDGE PC
1751 PINNACLE DRIVE
SUITE 500
MCLEAN, VA 22102-3833

EXAMINER	
LEE, CHUN KUAN	
ART UNIT	**PAPER NUMBER**
2181	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/04/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/808,287	KAMADA ET AL.	
	Examiner	Art Unit	
	Chun-Kuan (Mike) Lee	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 January 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

RESPONSE TO ARGUMENTS

1. Applicant's arguments filed 01/29/2007 have been fully considered but they are not persuasive. Currently, claims 2 is canceled and claims 1 and 3-5 are pending for examination.

2. In responding to applicant's arguments regarding that the combined teaching of Laine and Farazmandnia fail to teach/suggest the claimed limitation that "said direct memory access controller sets a number larger than the number of data received at a time as the number of transfers, and when the number of data transferred from said serial interface to said first memory reaches said number set as the number of transfers, said direct memory access controller outputs a direct memory access transfer end interrupt signal to a central processing unit," as stated on page 6, 1st paragraph. Applicant's arguments have fully been considered, but are not found to be persuasive.

Laine teaches the direct memory access (DMA) controller (Fig. 2, ref. 210) controlling the transferring of data between points in the memory space (e.g. FIFOs) without intervention of the CPU (col. 5, ll. 19-54), therefore it would have been obvious for the DMA controller to set parameters associated with the transferring of data, such as the size of the FIFO, as FIFO is utilized for the regulation of data transferring; and an interrupt generator (Fig. 3A, ref. 370) generating interrupts to the CPU according to the DMA configuration and state (col. 6, ll. 62-64), wherein it is well known for DMA

controller to send the interrupt to the CPU when the data request by the CPU has been completely transferred into the system memory for processing.

Farazmandnia teaches the buffering of data in the DMA FIFO (Fig. 2, ref. 204), wherein the data is transferred to the host memory (e.g. system memory) when the DMA FIFO is filled, wherein the DMA FIFO can be set to any size, but it is preferably to set the DMA FIFO to a size of 8 bytes, which is larger than the number of one byte data that is received at a time, as a number of transfers (col. 1, l. 52 to col. 2, l. 17), therefore when the number of one byte data that is received reaches the 8 bytes (i.e. DMA FIFO filled), data is transferred.

By combining Farazmandnia with Laine, the resulting combination of the references further teaches that the DMA controller controls the transferring of data between ports by setting the FIFO buffer (e.g. DMA FIFO) to the size of 8 bytes, which is larger than the number of one byte data that is received at a time, as the number of transfer, and when the number of one byte data that is received by the FIFO buffer reaches 8 bytes, the DMA controller send the interrupt to the CPU.

I. INFORMATION CONCERNING OATH/DECLARATION

Oath/Declaration

3. The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in **37 C.F.R. 1.63.**

II. INFORMATION CONCERNING DRAWINGS

Drawings

4. The applicant's drawings submitted are acceptable for examination purposes.

III. REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1 and 3-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Laine et al. (US Patent 6,687,796) in view of Farazmandnia et al. (US Patent 6,728,795).

6. As per claim 1, Laine teaches a serial communication device, comprising:

a serial interface (e.g. serial port) to receive data (col. 7, l. 66 to col. 8, l. 7); and

a direct memory access (DMA) controller (Fig. 2-3B, ref. 210) to transfer said data received by said serial interface from said serial interface to a first memory (e.g. first-in first-out (FIFO) buffer) (col. 5, ll. 36-54),

wherein said DMA controller is started up before said serial interface receives said data (col. 6, ll. 20-24), as the DMA controller's port must be able to respond to the

received request for data transferring, the DMA controller must be already active (i.e. already started up) before receiving the request;

wherein said DMA controller (Fig. 2, ref. 210) controls the transferring of data between points in the memory space (e.g. FIFOs) without intervention of the CPU (col. 5, ll. 19-54), therefore it would have been obvious for the DMA controller to set parameters associated with the transferring of data, such as the size of the FIFO, as FIFO is utilized for the regulation of data transferring, and

an interrupt generator (Fig. 3A, ref. 370) generating interrupts to the CPU according to the DMA configuration and state (col. 6, ll. 62-64), wherein it is well known for DMA controller to send the interrupt to the CPU when the data request by the CPU has been completely transferred into the system memory for processing.

Laine does not teach the serial communication device, comprising:

wherein said direct memory access controller sets a number larger than the number of data received at a time as the number of transfers; and

wherein when the number of data transferred from said serial interface to said first memory reaches said number set as the number of transfers, said direct memory access controller outputs a direct memory access transfer end interrupt signal to a central processing unit.

Farazmandnia teaches a system and a method comprising:

a universal serial asynchronous receiver transmitter (USART) (Fig. 2, ref. 200); and

receiving data through the USART and buffering of data in the DMA FIFO (Fig. 2, ref. 204), wherein the data is transferred to the host memory (i.e. system memory) when the DMA FIFO is filled, wherein the DMA FIFO can be set to any size, but it is preferably to set the DMA FIFO to a size of 8 bytes, which is larger than the number of one byte data that is received at a time, as a number of transfers (col. 1, l. 52 to col. 2, l. 17), therefore when the number of one byte data that is received reaches the 8 bytes (i.e. DMA FIFO filled), data is transferred.

Laine and Farazmandnia are analogous art because they are from same field of endeavor as both are associated with the DMA data transferring.

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Farazmandnia's transferring of data when the FIFO is filled into Laine's DMA controller. The resulting combination of the references further teaches the serial communication device comprising:

DMA controller setting to receive the data from the serial interface until the FIFO buffer (i.e. first memory) is fill (e.g. all 8 bytes within the FIFO buffer is filled), wherein the size of the FIFO buffer is lager than the number of data (e.g. one byte) received at a time; and

when the FIFO buffer is filled (i.e. first memory reaching the number set as the number of transfers by filling the FIFO buffer), data in the FIFO buffer is transferred to the host memory to be processed by the CPU, therefore along with the transferring of data to the host memory, the corresponding interrupt is also transferred to the CPU by the interrupt generator.

The suggestion/motivation for doing so would have been the implementation of high-speed asynchronous data transferring (Farazmandnia, col. 1, ll. 52-55).

Therefore, it would have been obvious to combine Farazmandnia with Laine for the benefit of implementing the high-speed asynchronous data transferring to obtain the invention as specified in claim 1.

7. As per claim 3, Laine and Farazmandnia teach all the limitations of claim 1 as discussed above, where Farazmandnia further teaches the serial communication device comprising wherein said serial interface outputs a receive timeout interrupt signal to said central processing unit when said data reception is stopped for a certain period after the start of said data reception (Farazmandnia, col. 2, ll. 1-17), wherein the transferring of data from the FIFO buffer to the host memory is resulted from a timer expiring, which would also initiate the corresponding transferring of interrupt to the CPU.

8. As per claim 4, Laine and Farazmandnia teach all the limitations of claim 3 as discussed above, where Farazmandnia further teaches the serial communication device comprising wherein said direct memory access controller retransfers said transferred data from said first memory (Farazmandnia, DMA buffer 204 of Fig. 2) to a second memory (Farazmandnia, host memory 208 of Fig. 2) as triggered by said direct memory access transfer end interrupt signal or said receive timeout interrupt signal (Farazmandnia, col. 1, l. 52 to col. 2, l. 17).

9. As per claim 5, Laine and Farazmandnia teach all the limitations of claim 1 as discussed above, where both further teach the serial communication device comprising

wherein said first memory is comprised of two or more memory areas (Laine, FIFO 0, FIFO 1, FIFO 2, FIFO 3, FIFO 4, FIFO 5 of Fig. 3A), and

wherein said direct memory access controller has a continuous transfer function and transfers said data from said serial interface to said first memory while alternately switching the destinations of the data received by said serial interface among said two or more memory areas as triggered by said direct memory access transfer end interrupt signal or a receive timeout interrupt signal (Laine, col. 16, ll. 49-57 and Farazmandnia, col. 1, l. 52 to col. 2, l. 17), wherein the DMA controller is a multi-channel DMA controller and servicing each corresponding channels in a round-robin method, therefore, in finishing the servicing of one of the channels, the multi-channel DMA controller switches to receiving data for the next channel into the corresponding FIFO buffer, wherein the servicing finished either from the filling of the FIFO buffer or the expiration of the timer.

IV. CLOSING COMMENTS

Conclusion

a. STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. 707.07(i)**:

a(1) CLAIMS REJECTED IN THE APPLICATION

Per the instant office action, claims 1 and 3-5 have received a first action on the merits and are subject of a first action non-final.

b. DIRECTION OF FUTURE CORRESPONDENCES

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun-Kuan (Mike) Lee whose telephone number is (571) 272-0671. The examiner can normally be reached on 8AM to 5PM.

IMPORTANT NOTE

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

April 2, 2007

Chun-Kuan (Mike) Lee
Examiner
Art Unit 2181

DONALD SPARKS
SUPERVISORY PATENT EXAMINER